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10/717,970	11/21/2003	Yoshifumi Tanada	12732-178001 / US6774	8011

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EXAMINER

SHERMAN, STEPHEN G

ART UNIT	PAPER NUMBER
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2629

DATE MAILED: 06/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/717,970

Applicant(s)

TANADA ET AL.

Examiner

Stephen G. Sherman

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 August 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 August 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 3-16-04/16-2204
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Drawings

1. Figures 5A-5B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 7 and 13 recite the limitation "pixel electrodes." There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1 and 19-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Tokimoto et al. (EP 1 204 087 A1).

Regarding claim 1, Tokimoto et al. disclose a display device including pixels that include first to n-th (where n is a natural number, $2 \leq n$) light-emitting elements that emit different emission colors (Figure 7 shows the configuration of a pixel which includes light emitting elements 11, 12 and 13 which emit red, green and blue color.), wherein any one of the first to n-th light-emitting elements is sequentially selected and emits light (Figure 8 and paragraphs [0058]-[0059] explain that the red, green and blue LEDs are selected sequentially in order to emit light.).

Regarding claim 19, Tokimoto et al. disclose a driving method of a display device comprising the steps of:

sequentially selecting any one of first to n-th (where n is a natural number, $2 \leq n$) light-emitting elements that are included in pixels and emit different emission colors (Figure 8 and paragraphs [0058]-[0059] explain that the red, green and blue LEDs are selected sequentially.);

controlling potential between two electrodes of the selected light-emitting element (Paragraph [0057] explains that the two electrodes of the LEDs are connected between a current source and a power source and that a switch controls the connection to the power source Vcc in order to control the potential between the two electrodes of the LED.); and

sequentially causing the light-emitting element to emit light (Figures 7 and 8 and paragraphs [0057]-[0059] explain that the red, green and blue LEDs sequentially emit light.).

Regarding claim 20 (with respect to claims 1 and 19), Tokimoto et al. disclose an electronic apparatus using the display device according to claim 1 or the driving method of the display device of claim 19 (Paragraph [0020]).

6. Claims 3-6, 9-12, 15-18 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Knapp et al. (US 2003/0117348).

Regarding claim 3, Knapp et al. disclose a display device comprising:

first to $(n+1)$ th (where n is a natural number, $2 \leq n$) pixel electrodes and first to n -th light-emitting elements that are disposed so as to be sandwiched between the first to $(n+1)$ th pixel electrode portions and emit different emission colors (Figure 4 shows display elements 11a-11c which have pixel electrodes on either side of the light emitting elements such that 11a emits red light, 11b emits blue light and 11c emits green light.);

a transistor for switching (Figure 4, transistor 16);

pixels including first to n -th transistors for driving (Figure 4, transistors 21-22.

The examiner interprets from paragraphs [0064]-[0065] and [0071] that the shunt transistors 22 work in conjunction with the driving transistor 12 to drive the display elements 11a-11c, therefore making the transistors drive transistors used for driving the display.);

a source signal line (Figure 4, data line 17);

a gate signal line (Figure 4, gate line 15);

first to n -th current supply lines (Figure 4, control lines 23 are explained to carry current in paragraph [0065].)); and

a power line (Figure 4, item 21);

wherein:

a gate electrode of the transistor for switching is electrically connected to the gate signal line (Figure 4, the gate of transistor 16 is connected to gate line 15.),

a first electrode of the transistor for switching is electrically connected to the source signal line (Figure 4, the transistor 16 is connected to the data line 17.),

a second electrode of the transistor for switching is electrically connected to gate electrodes of the first to n-th transistors for driving (Figure 4, the transistor 16 is connected to the gate of driving transistor 12 which is in turn connected to the gates of transistors 22.),

the m-th (where m is a natural number, $1 \leq m \leq n$) pixel electrode is electrically connected to the m-th current supply line via the m-th transistor for driving (Figure 4 shows that display elements 11a-11c are connected to the current supply lines 23 through transistors 22.), and

the (n+1)th pixel electrode is electrically connected to the power line (Figure 4 shows that display element 11c has a last electrode connected to the power source 21.).

Regarding claim 4, Knapp et al. disclose The display device according to claim 3, further comprising:

a gate signal line for erasure (Figure 4, gate line 15 also acts as a gate line for erasure.); and

a transistor for erasure (Figure 4, transistors 24 are transistors for erasure.);

wherein:

the gate electrode of the transistor for erasure is electrically connected to the signal line for erasure (Figure 4 shows that the gate of transistor 24 is connected to the gate line 15.),

the first electrode of the transistor for erasure is electrically connected to the gate electrodes of the first to n-th transistors for driving (Figure 4 shows that the transistors 24 are connected to the gates of transistors 22.), and

the second electrode of the transistor for erasure is electrically connected to any one of the first to n-th current supply lines (Figure 4 shows that transistors 24 are connected to the lines 23.).

Regarding claim 5, Knapp et al. disclose the display device according to claim 3, further comprising:

a gate signal line for erasure (Figure 4, gate line 15 also acts as a gate line for erasure.);

a transistor for erasure (Figure 4, transistors 42 are transistors for erasure.); and

a retention volume line (Figure 4, item 41.);

wherein:

the gate electrode of the transistor for erasure is electrically connected to the gate signal line for erasure (Figure 4 shows that the gate electrode of transistor 42 is connected to gate line 15.),

the first electrode of the transistor for erasure is electrically connected to the gate electrodes of the first to n-th transistors for driving (Figure 4 shows that the transistors 42 are connected to the gates of transistors 22 through capacitors 43.), and

a second electrode of the transistor for erasure is electrically connected to the

retention volume line (Figure 4 shows that the transistors 42 are connected to the line 41.).

Regarding claim 6, Knapp et al. disclose the display device according to claim 3, further comprising:

a gate signal line for erasure (Figure 4, gate line 15 also acts as a gate line for erasure.); and

first to n-th transistors for erasure (Figure 4, transistors 42 are transistors for erasure.);

wherein:

the gate electrodes of the first to n-th transistors for erasure are electrically connected to the gate signal line for erasure (Figure 4 shows that the gate electrode of transistor 42 is connected to gate line 15.), and

the first to n-th transistors for erasure are disposed between the first to n-th pixel electrodes and the first to n-th transistors for driving (Figure 4 shows that transistors 42 are disposed between driving transistor 12 and elements 11a-11c.).

Regarding claims 9-12, Knapp et al. disclose the display device according to claims 3-6, wherein the second to n-th pixel electrodes all comprise a transparent substance (It would be inherent to make the pixel electrodes comprise a transparent substance.).

Regarding claims 15-18, Knapp et al. disclose the display device according to claims 9-12, wherein the first to n-th light-emitting elements and the first to (n+1)th pixel electrodes are laminated (It would be inherent for the light emitting elements and pixel electrodes to be laminated.).

Regarding claim 20 (with respect to claims 3-6, 9-12 and 15-18), Knapp et al. disclose an electronic apparatus using the display device according to any one of claims 3-6, 9-12 and 15-18 (Figure 7 and paragraph [0040].).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 2, 8, 14 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitakado et al. (JP 2002-297083 A) in view of Kondo et al. (JP 2002-287664 A).

Regarding claim 2, Kitakado et al. disclose a display device comprising:

- first to $(n+1)$ th (where n is a natural number, $2 \leq n$) pixel electrodes (Drawings 6 and 8 and paragraph [0041]);
- first to n -th light-emitting elements that are disposed so as to be sandwiched between the first to $(n+1)$ th pixel electrodes and emit different emission colors (Drawings 6 and 8 and paragraph [0041]);
- pixels including first to n -th transistors for driving (Drawing 6 and 8 show transistors 16b.);
- a current supply line (Drawing 8 shows current supply line 21 as explained in paragraph [0041].); and
- a power line (Figure 8 shows power line 24(B) which is explained in paragraph [0042] to hold a potential, i.e. voltage.);

wherein:

- the m -th (where m is a natural number, $1 \leq m \leq n$) pixel electrode is electrically connected to the current supply line via the m -th transistor for driving (Figure 8 shows that each transistor 16b is electrically connected to the current supply line 21 and the pixel electrodes 17.),

the (n+1)th pixel electrode is electrically connected to the power line (Figure 8 shows that the last pixel electrode is connected to the power source line 24(B).), and the potential difference between the pixel electrodes sandwiching the m-th light-emitting element is sequentially adjusted so that the m-th light-emitting element selectively emits light (Paragraph [0042].).

Kitakado et al. fails to teach of first to n-th current supply lines, where the m-th (where m is a natural number, $1 \leq m \leq n$) pixel electrode is electrically connected to the m-th current supply line via the m-th transistor for driving.

Kondo et al. disclose of a display device with first to n-th current supply lines, where the m-th (where m is a natural number, $1 \leq m \leq n$) pixel electrode is electrically connected to the m-th current supply line via the m-th transistor for driving (Drawings 6 and 9 show that each color may have its own current source which is supplied to the pixel circuit, where the pixel electrode would be connected to the current source through a driving transistor as explained in paragraphs [0053] and [0057].).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to provide for a separate current supply line for each color as taught by Kondo et al. to replace the single current supply line in the display device taught by Kitakado et al. in order to eliminate the need for a switching output by a current regulator circuit, which results in less power consumption by the device.

Regarding claim 8, Kitakado et al. and Kondo et al. disclose the display device according to claim 2, wherein the second to n-th pixel electrodes all comprise a

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transparent substance (It would be inherent to make the pixel electrodes comprise a transparent substance.).

Regarding claim 14, Kitakado et al. and Kondo et al. disclose the display device according to claim 8, wherein the first to n-th light-emitting elements and the first to (n+1)th pixel electrodes are laminated (It would be inherent for the light emitting elements and pixel electrodes to be laminated.).

Regarding claim 20 (with respect to claims 2, 8 and 14), Kitakado et al. and Kondo et al. disclose an electronic apparatus using the display device according to any one of claims 2 8 and 14 or the driving method of the display device of claim 19 (Kondo et al. paragraph [0001].).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ouchi et al. (US 2003/0107537) discloses a current driving matrix display involving the driving of individual colors in a pixel.

Hiyama et al. (US 6,909,442) discloses a display device where each pixel comprises a red, green and blue display element.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

2 June 2006



RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

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